WHAT IS CLAIMED IS:

1. An information data recording apparatus for recording information data on an information recording medium having pre-pits which are formed at periodic intervals having a period that is m, m being an integer, times as large as a unit period in accordance with pre-information recorded at an interval which deviates from said periodic intervals by an interval that is k, k being an integer, where $k < m$, times said unit period in accordance with recording positions, said apparatus comprising:

a unit period signal generator which generates a periodic signal of said unit period;

a memory for temporarily storing said information data in synchronism with said periodic signal from said unit period signal generator and supplying said information data in synchronism with a clock signal;

a pre-pit signal reproducing circuit for detecting said pre-pits from said recording medium and generating a pre-pit signal;

a phase-locked loop circuit for generating said clock signal which is phase-locked with a jitter component contained in said pre-pit signal; and

a recording means for recording said information data supplied from said memory on said recording medium.

2. An information data recording apparatus as claimed in claim 1, wherein said phase-locked loop circuit comprises:

a voltage controlled oscillator for generating said clock signal in accordance with a control voltage;

a phase comparator circuit for comparing said pre-pit signal generated by said pre-pit signal reproducing circuit with said clock signal generated by said voltage controlled oscillator and producing a phase comparison output signal; and

an amplitude and phase equalizing circuit for adjusting amplitude and phase of said phase comparison output signal of said phase comparator to produce said control voltage supplied to said voltage controlled oscillator.

3. An information data recording apparatus as claimed in claim 1, further comprising a feed-forward circuit for eliminating a phase error in said information data supplied from said memory, said phase error corresponding to a residual phase error component of said clock signal generated by said phase-locked loop circuit.

4. An information data recording apparatus as claimed in claim 3, wherein said feed-forward circuit comprises:

a second memory for storing said information data supplied from said memory in synchronism with said clock

43

signal and supplying said information data to said recording means in synchronism with a second clock signal; and

a voltage controlled oscillator for generating said second clock signal in accordance with said phase comparison output signal of said phase comparator circuit.